WHAT IS CLAIMED IS:

1. An arithmetic unit with a reduced startup time having a CPU, a cache for storing cache data, a RAM, and a non-volatile memory, the arithmetic unit comprising:

determination means for determining whether data to be read by the CPU is in the RAM;

a switching device for allowing the CPU to directly read the data from the non-volatile memory, depending on a result of determination by the determination means; and

a cache controller for controlling the cache so that the RAM is initialized based on the cache data corresponding to the data.

2. The arithmetic unit with a reduced startup time according to claim 1, wherein the determination means makes the determination by referring to a RAM data determination bit table which retains information concerning the presence or absence of data in the RAM.

3. The arithmetic unit with a reduced startup time according to claim 1, wherein the switching device has a function of determining, if the data is not in the RAM, an address in the non-volatile memory that corresponds to the data.

4. The arithmetic unit with a reduced startup time according to claim 1, wherein the cache controller has a function of setting, if the data is stored in the cache as cache data, all dirty bits of cache tags associated with the cache data to "dirty".

5. The arithmetic unit with a reduced startup time according to claim 1, wherein the cache controller has a function of writing, if the data is stored in the cache as cache data, to a cache tag associated with the cache data an address in the RAM that corresponds to the cache data.

6. The arithmetic unit with a reduced startup time according to claim 1, wherein the non-volatile memory is a ROM.

7. A method of loading data in an arithmetic unit having a CPU, a cache, a RAM, and a non-volatile memory, the method comprising:

determining whether data to be read by the CPU is in the RAM;

allowing the CPU to directly read the data from the non-volatile memory, depending on a result of the determination; and

controlling the cache so that the RAM is initialized based on cache data corresponding to the data stored in the cache when read directly by the CPU from the non-volatile memory.